DDA-08/16 Register-Level Programming

USER'S GUIDE

DDA-08/16 Register-Level Programming User's Guide

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Preface

This guide describes the register-level functions of the DDA-08 and DDA-16 boards and is offered as a supplement to the *DDA-08/16 User's Guide*. Unless this guide refers specifically to the DDA-08 or DDA-16 board, it refers to both boards collectively as the DDA-08/16 boards.

The *DDA-08/16 Register-Level Programming User's Guide* is intended for users whose applications require operational control other than what is provided by the software packages currently available for DDA-08/16 boards. To use the information in this manual, you must be familiar with data acquisition principles and with the functions of the DDA-08/16 boards. You must also be familiar with the configuration and installation requirements for DDA-08/16 boards, and you must be experienced at programming register-level functions.

Note: The information in this guide is not intended for use with any of the software packages currently available for DDA-08/16 boards. If you want information on a particular software package, refer to the manual for that package.

This guide is organized as follows:

- Chapter 1 describes the functions for each I/O address of the DDA-08/16 boards.
- Chapter 2 outlines an example procedure for programming DDA-08/16 boards to enable the analog outputs.
- Appendix A summarizes functions of the bits at each I/O address of the DDA-08/16 boards.

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I/O Addresses

DDA-08/16 boards use eight addresses in the computer I/O space. The addresses start at the base address and extend as shown in the I/O map of Table 1-1.

Table 1-1. I/O Address Map

Location	Function	Type
Base Address +0h	Register for pacer and output clock counters Register for data to analog output channel	Read/write Write-only
Base Address + 1h	Register for data to analog output channel	Write-only
Base Address +2h	Data Pointer register for indirect address pointer to data	Read/write
Base Address +3h	Not used	—
Base Address +4h	Board Control/Status register	Read/write
Base Address +5h	Channel Control/Status register	Read/write
Base Address +6h	Status Pointer register for indirect address pointer to control/status	Read/write
Base Address +7h	Not used	—

The following sections describe the I/O address map in more detail.

Base Address +0h and +1h

Base Address +0h and Base Address +1h each address a separate 8-bit register. The use of these two registers depends on the setting of DP4 in the register at Base Address +2h. When DP4 = 0, the two registers become write-only for data writes to a specified analog output channel. When DP4 = 1, the register at Base Address +0h becomes read/write for loading or reading of a specified counter, while the register at Base Address +1h goes unused. Refer to page 1-3 for more information on the register at Base Address +2h.

As Registers for Data to the Analog Output Channel

When DP4 of Base Address +2h equals 0, Base Address +0h becomes write-only and has the following bit assignments:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

When DP4 of Base Address +2h equals 0, Base Address +1h becomes write-only and has the following bit assignments:

7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8

As the bit assignments indicate, the specified 12-bit analog output loads as two 8-bit bytes of data. The eight least significant bits of data load into Base Address +0h, and the four most significant bits of data load into the low nibble (bit 0 to bit 3) of Base Address +1h. The X signifies *unused*. If an analog output channel is not a member of the update group, the channel updates when the top four bits are written.

The code you use to represent an analog output value depends on whether you are using a bipolar or unipolar output range type, as follows:

- For bipolar output signal ranges, the analog output value is represented in offset binary format. A code of 0000 0000 0000 represents negative full scale, a code of 1111 1111 1111 represents positive full scale, and a code of 1000 0000 0000 represents 0 V.

- For unipolar output signal ranges, the analog output value is represented in binary format. A code of 0000 0000 0000 represents 0 V and a code of 1111 1111 1111 represents positive full scale.

As Registers for the Pacer and Output Clock Counters

When DP4 of Base Address +2h equals 1, Base Address +0h becomes read/write and has the following bit assignments:

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

When DP4 of Base Address +2h equals 1, Base Address +1h is unused.

As the bit assignments indicate, the register at Base Address +0h writes data to the pacer clock counter or the output clock counter. Refer to “As Miscellaneous Status Register” on page 1-8 for information on setting the frequency associated with the counters. The pacer clock counter counts down the frequency of the board clock. The count is one more than the value loaded in the counter. If the clock is 1 kHz and the count is zero, the frequency is 1 kHz. Reading the clock while it is running shows the remaining counts in the current cycle. The output clock counter determines the delay between an update and the output clock pulse. Loading a zero means the output clock pulse occurs immediately following the update. Reading the output clock counter indicates the number of counts remaining between the update event and the output clock. Refer to “As Run Status Register” on page 1-5 for information on controlling these counters.

Base Address +2h

Base Address +2h is is read/write and is the location for the indirect address pointer to data (Data Pointer) register. The settings of this register determine how you use the registers at Base Address +0h and +1h. Bit assignments for Base Address +2h are as follows:

7	6	5	4	3	2	1	0
X	X	X	DP4	DP3	DP2	DP1	DP0

Definitions for the bit names are as follows:

- **X** - not used.
- **DP4** - Data Pointer bit 4 determines the use of registers at Base Address +0h and +1h as follows:
  - If DP4 = 0, the registers at Base Address +0h and +1h handle data writes to the analog output channel specified by bits DP3 to DP0 of Base Address +2h.
  - If DP4 = 1, the register at Base Address +0h handles read/writes to the counter specified by bit 0 of Base Address +2h.
- **DP3 to DP0** - Data Pointer bits 3 to 0 function according to the setting of DP4 as follows:
  - If DP4 = 0, the board decodes settings of DP3 to DP0 to determine which analog output channel the data in the registers at Base Address +0h and +1h is written to. For example, DP3 to DP0 settings of 0000 select channel 0, settings of 0001 select channel 1, and so on up to 1111 for channel 15.

Note: The DDA-08 decodes bit DP3 as 0, so that (for example) 1111 and 0111 are both decoded as 7.

If the SEQ bit of the Board Status register (page 1-6) is set, the data pointer automatically increments to the next channel after a write of the high data byte. The selected DDA channel returns to zero after a write to channel 15.

Note: On a DDA-08 board, the data pointer sequences from 0 to 15, but the hardware decode logic treats bit DP3 as 0, keeping the DDA channel sequencing at 0 to 7. Thus, while the data pointer on the DDA-08 board sequences from 0 to 15, the DDA channel is sequencing from 0 to 7 twice.

  - If DP4 = 1, the setting of DP0 determines which counter loads the data written to Base Address +0h and +1h. A setting of DP0 = 0 selects the pacer clock counter; a setting of DP0 = 1 selects the output clock counter.

Base Address +4h

Base Address +4h serves as one of four read/write status registers, depending on the settings of bits SP1 and SP0 of the Status Pointer register (Base Address +6h). The following subsections describe each of the status registers at Base Address +4h.

As Run Status Register

To select the Run Status register, set bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) as follows: SP1 = 0; SP0 = 0. Bit assignments for the Run Status register are as follows:

7	6	5	4	3	2	1	0
TRE	GAE	OTR	OON	RCT	X	SWT	UPD

Definitions for the bit names are as follows:

- **TRE** - Setting this bit enables the trigger input
- **GAE** - Setting this bit enables the gate input
- **OTR** - This bit indicates whether the output timer is on (read only) as follows:
  - 0 = Off
  - 1 = On
- **OON** - Setting this bit enables output clock generation
- **RCT** - This bit enables/disables the onboard periodic pacer clock timer as follows: 0 = disables, 1 = enables
- **X** - Not used; ignored on write, 0 when read
- **SWT** - Writing this bit initiates an analog output update for analog output channels in the update group; 0 when read

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Note: Before writing SWT, you must set bits CS1 and CS0 of the Clock Select register to 1, selecting the software trigger.

- **UPD -** This bit (read only) indicates whether the analog output channels are updated, as follows:
  - 0 = Not updated
  - 1 = Updated

  A read automatically clears this bit.

As Board Status Register

To select the Board Status register, set bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) as follows: SP1 = 0, SP0 = 1. Bit assignments for the Board Status register are as follows:

7	6	5	4	3	2	1	0
X	X	X	DOE	SEQ	IL2	IL1	IL0

Definitions for the bit names are as follows:

- **X** - Not used; ignored on write, 0 when read
- **DOE** - Setting this bit enables the analog outputs

Note: Load the input buffers of the analog output channels with appropriate values before setting the DOE bit (see Example 1 on page 2-1).

- **SEQ** - Setting this bit enables automatic incrementing of the analog output channel specified by Base Address +2h
- **IL2 to IL0** - These bits select the interrupt level as follows:
  - 000 = Interrupt disabled (power up)
  - 001 = Level 3
  - 010 = Level 5
  - 011 = Level 7
  - 100 = Level 10
  - 101 = Level 11

- 110 = Level 15
- 111 = Not used

As Clock Select Register

To select the Clock Select register, set bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) as follows: SP1 = 1, SP0 = 0. Bit assignments for the Clock Select register are as follows:

7	6	5	4	3	2	1	0
X	X	OP	TRP	GAP	CP	CS1	CS0

Definitions for the bit names are as follows:

- **X** - Not used; ignored on write, 0 when read
- **OP** - This bit selects the output clock polarity as follows:
  - 0 = High-to-low edge
  - 1 = Low-to-high edge
- **TRP** - This bit selects trigger polarity as follows:
  - 0 = High-to-low edge enables clocks
  - 1 = Low-to-high edge enables clocks
- **GAP** - This bit selects gate polarity as follows:
  - 0 = Enables low gate
  - 1 = Enables high gate
- **CP** - This bit selects the external pacer clock polarity as follows:
  - 0 = High-to-low edge
  - 1 = Low-to-high edge
- **CS1, CS0** - These bits select the clock source as follows:
  - 00 = Disabled (power up)
  - 01 = Onboard clock
  - 10 = External clock
  - 11 = Software

As Miscellaneous Status Register

To select the Miscellaneous Status register, set bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) as follows: SP1 = 1, SP0 = 1. Bit assignments for the Miscellaneous Status register are as follows:

7	6	5	4	3	2	1	0
PS2	PS1	PS0	X	CLI	GAI	TR1	8/16

Definitions for the bit names are as follows:

- **PS2 to PS0** - These bits select the value of prescaler clock frequency/period as follows:
  - 000 = 1 Hz (power up); 1 s
  - 001 = 10 Hz; 100 ms
  - 010 = 100 Hz; 10 ms
  - 011 = 1 kHz; 1 ms
  - 100 = 10 kHz; 100 µs
  - 101 = 100 kHz; 10 µs
  - 110 = 1 MHz; 1 µs
  - 111 = Not used
- **X** - Not used; ignored on write, 0 when this bit is read
- **CLI** - Indicates clock input line level (read only), as follows:
  - 0 = Low
  - 1 = High
- **GAI** - Indicates gate input line level (read only), as follows:
  - 0 = Low
  - 1 = High
- **TRI** - Indicates trigger input line level (read only), as follows:
  - 0 = Low
  - 1 = High

- **8/16** - This bit is read only and indicates the type of board, as follows:
  - 0 = 16-channel
  - 1 = 8-channel

Base Address +5h

Base Address +5h serves as one of four status registers for the quad DACs, depending on the settings of bits SP1 and SP0 of the Status Pointer register (Base Address +6h). Two of these registers contain the control/status information for the quad DACs, and two registers contain the status of the current/voltage select switch for all channels. The following subsections describe each of the status registers for the quad DACs.

As Control/Status Register for Quad DACs 0 and 1

This register is read/write and holds values for quad analog outputs 0 and 1 of the DDA-08 and DDA-16 boards. To select this register, set bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) as follows: SP1 = 0, SP0 = 0. Bit assignments for the Control/Status register for quad DACs 0 and 1 are as follows:

7	6	5	4	3	2	1	0
TG1	SP11	SP10	U/B1	TG0	SP01	SP00	U/B0

Definitions for the bit names are as follows:

- **TG1** - Setting this bit puts quad DAC 1 in the update group (power-up value = 0)
- **SP11, SP10** - These bits (read only) are determined by board switch S6 and indicate the output span of quad DAC 1, as follows:
  - 10 = 5 V span or current output
  - 01 = 10 V span
  - 11 = 20 V span

- **U/B1** - This bit (read only) is determined by board switch S2 and indicates the output range type of quad DAC 1 as follows:
  - 0 = Unipolar or current output
  - 1 = Bipolar
- **TG0** - Setting this bit puts quad DAC 0 in the update group (power-up value = 0)
- **SP01, SP00** - These bits (read only) are determined by board switch S5 and indicate the output span of quad DAC 0 as follows:
  - 10 = 5 V span or current output
  - 01 = 10 V span
  - 11 = 20 V span
- **U/B0** - This bit (read only) is determined by board switch S1 and indicates the output range type of quad DAC 0 as follows:
  - 0 = Unipolar or current output
  - 1 = Bipolar

As Control/Status Register for Quad DACs 2 and 3

This register holds values for quad DACs 2 and 3 of the DDA-16 boards only. To select this register, bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) must be set as follows: SP1 = 0, SP0 = 1. Bit assignments for the Control/Status register for quad DACs 2 and 3 are as follows:

7	6	5	4	3	2	1	0
TG3	SP31	SP30	U/B3	TG2	SP21	SP20	U/B2

Definitions for the bit names are as follows:

- **TG3** - Setting this bit puts quad DAC 3 in the update group (power-up value = 0)
- **SP31, SP30** - These bits (read-only) are determined by board switch S8 and indicate the output span of quad DAC 3, as follows:
  - 10 = 5 V span or current output
  - 01 = 10 V span

  - 11 = 20 V span

- **U/B3 -** This bit (read-only) is determined by board switch S4 and indicates the output range type of quad DAC 3, as follows:
  - 0 = Unipolar or current output
  - 1 = Bipolar
- **TG2 -** Setting this bit puts quad DAC 2 in the update group (power-up value = 0)
- **SP21, SP20 -** These bits (read-only) are determined by board switch S7 and indicate the output span of quad DAC 2, as follows:
  - 10 = 5 V span or current output
  - 01 = 10 V span
  - 11 = 20 V span
- **U/B2 -** This bit (read-only) is determined by board switch S3 and indicates the output range type of quad DAC 2, as follows:
  - 0 = Unipolar or current output
  - 1 = Bipolar

Normally, you set the TG bits during initialization to define the update group. A read of this register determines the output range of each quad DAC. If you select a 20 V span for unipolar mode, the analog output does not work correctly and the Function Call Driver returns an error.

As Current/Voltage Switch Status Register for Channels 0 to 7

This register is read-only and holds values representing the settings of the current/voltage select switches (board switches S10 to S17) for channels 0 to 7 of the DDA-08 and DDA-16 boards. To select this register, bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) must be set as follows: SP1 = 1, SP0 = 0. Bit assignments for this register are as follows:

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

These bits represent the current/voltage setting for each channel as follows: 0 = current output, 1 = voltage output

As Current/Voltage Switch Status Register for Channels 8 to 15

This register is read-only and holds values representing the settings of the current/voltage select switches (board switches S18 to S25) for channels 8 to 15 of the DDA-16 boards only. To select this register, bits SP1 and SP0 of the Status Pointer register (at Base Address +6h) must be set as follows: SP1 = 1, SP0 = 1. Bit assignments for this register are as follows:

7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8

These bits represent current/voltage setting for each channel as follows: 0 = current output; 1 = voltage output

Base Address +6h

Base Address +6h is the location for the indirect address pointer to the control/status registers. The settings of the register at Base Address +6h determine which of the control/status registers is read/written. Bit assignments for Base Address +6h are as follows:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	SP1	SP0

Definitions for the bit names are as follows:

- **X** - not used.

- **SP1, SP0** - Status pointer bits SP1 and SP0 select a register at Base Address +4h as follows:
  - 00 = Run Status register at Base Address +4h for board control/status
  - 01 = Board Status register at Base Address +4h for board control/status
  - 10 = Clock Select register at Base Address +4h for board control/status
  - 11 = Miscellaneous Status register at Base Address +4h for board control/status

  Status pointer bits SP1 and SP0 select a register at Base Address +5h as follows:
  - 00 = Control/Status register at Base Address +5h for quad DACs 1 and 0
  - 01 = Control/Status register at Base Address +5h for quad DACs 3 and 2
  - 10 = Current/Voltage Select register at Base Address +5h for channels 0 to 7
  - 11 = Current/Voltage Select register at Base Address +5h for channels 8 to 15

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Programming Examples

This chapter provides basic steps for programming a DDA-08/16 to initialize and enable the analog outputs.

Example 1: Initialize and Enable the Analog Outputs

The following two examples describe how to initialize and enable the analog outputs.

Initialize the Analog Outputs

You initialize the outputs to load data corresponding to 0 V one-at-a-time, as follows:

- Initialize channel 0 by writing 12-bit word data to bits 0 to 7 of Base Address +0h and bits 0 to 3 of Base Address +1h, as follows:
  - If the board is set (by onboard switches) for unipolar, write 00000000 to Base Address +0h and 0000 to Base Address +1h.
  - If the board is set (by onboard switches) for bipolar, write 11111111 to Base Address +0h and 0111 to Base Address +1h.
- Initialize subsequent channels as follows:

1. Write a binary number to Base Address +2h to set Base Address +0h and +1h for channel *n*. For example, write 0001 for channel 1, 0010 for channel 2, and so on.
2. Initialize channel *n* by writing 12-bit word data to bits 0 to 7 of Base Address +0h and to bits 0 to 3 of Base Address +1h.

– If the board is set by board switches for unipolar, write 00000000 to Base Address +0h and 0000 to Base Address +1h.

– If the board is set by board switches for bipolar, write 11111111 to Base Address +0h and 0111 to Base Address +1h.

Enable the Analog Outputs

Use the following steps to enable the analog outputs:

1. Write 01 to Base Address +6h to select the Board Status register at Base Address +4h.
2. Write to Base Address +4h to set bit 4 (DOE), enabling the analog outputs to 0.000 volts.

Example 2: Generate a Square Wave on Channel 0

Before performing the following test-routine procedure, you must initialize and enable the analog outputs using the procedures under “Example 1: Initialize and Enable the Analog Outputs” on page 2-1.

1. Write 00 to Base Address +6h to select the Run Status register at Base Address +4h.
2. Write 00010000 to the Run Status register (Base Address +4h) to turn off both clocks.
3. Write 00010000 to the data pointer (Base Address +2h) to select the output of the pacer clock counter.
4. Write 01101110 to the register (Base Address +0h) to set the output of the pacer clock counter to 110.
5. Write 00010001 to the data pointer (Base Address +2h) to select the output of the output clock counter.
6. Write 00000000 to the register at Base Address +0h to zero the output of the output clock counter, making the output clock occur almost simultaneously with the pacer clock.
7. Write 11 to Base Address +6h to select the Miscellaneous Status, register at Base Address +4h.

8. Write 11000000 to the Miscellaneous Status register (Base Address +4h) to set the prescaler frequency for 1 MHz which, when combined with the value in Step 4, gives a period of 110 µs.
9. Write 00 to Base Address +6h to select the Control/Status register (Base Address +5h) for quad DACs 0 and 1.
10. Write 00001000 to the Control/Status register (Base Address +5h) to put quad DAC 0 in the update group (with a power-up value of 0).
11. Write 10 to Base Address +6h to select the Clock Select register at Base Address +4h.
12. Write 00000001 to the Clock Select register (Base Address +4h) to select the onboard pacer clock as the clock source.
13. Write 00 to Base Address +6h to select the Run Status register at Base Address +4h.
14. Write 00011000 to the Run Status register (Base Address +4h) to enable the output clock timer and the pacer clock timer.
15. Write 00000000 to the data pointer register (Base Address +2h) to select analog output channel 0.
16. Write 11111111 to Base Address +0h and 00001111 to Base Address +1h (at the next update, analog output channel 0 changes to maximum value; the actual value depends on whether the channel is set for unipolar or bipolar).
17. Read the Run Status register (Base Address +4h) until bit 0 (UPD) sets, indicating that analog output channel 0 is updated.

Note: Reading the UPD bit automatically clears it.

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18. Write 00000000 to Base Addresses +0h and +1h to set these registers for the next change (at the next update, analog output channel 0 changes to the minimum value; the actual value depends on whether the channel is set for unipolar or bipolar).

19. Again, read the Run Status register (Base Address +4h) until bit 0 (UPD) sets, indicating that analog output channel 0 is updated.

Note: Reading the UPD bit automatically clears it.

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20. Repeat Steps 16 to 19 for each waveform cycle you wish to add to your series of square waves.

Example 3: Use the Interrupts

The following two subsections contain the procedures required to enable the interrupt process.

Initializing the Interrupt Process

The following procedure enables the generation of an interrupt for every period of the pacer clock.

1. Install the interrupt handler in memory.
2. Enable and reset each of the four status registers (Base Address +4h) by writing the appropriate binary number to Base Address +6h and writing zero to the register.
3. Enable the Miscellaneous Status register (Base Address +4h) by writing 11 to Base Address +6h.
4. Write to the Miscellaneous Status register to set the desired prescaler value.
5. Write 1000 to Base Address +2h to enable Base Address +0h for read/writes to the pacer clock counter.
6. Write to Base Address +0h to set the desired rate for pacer clock update.
7. Enable the Board Status register (Base Address +4h) by writing 01 to Base Address +6h.
8. Write to the Board Status register to select the desired interrupt level.
9. Enable the Clock Select register (Base Address +4h) by writing 10 to Base Address +6h.

10. Write 01 to the Clock Select register to select the onboard pacer clock.
11. Write to Base Address +2h to set up the data registers (Base Addresses 0h and 1h) to handle analog output data and to specify the desired analog output channel.
12. Write the data to be output by the desired analog output channel to the data registers at Base Address +0h and Base Address +1h.
13. Enable the PC interrupt for the interrupt level selected in Step 8.
14. Write 00 to Base Address +6h to enable the Run Status register (Base Address +4h).
15. Write to the Run Status register to set the RCT bit (bit 3) to start the clock.

Determining the Source of an Interrupt

The following procedure is contained in the Interrupt Service Routine (already installed in memory); the procedure determines the source of an interrupt and updates the appropriate board. The procedure also assumes that the DDA-08/16 board or boards in your PC are initialized according to the preceding procedure.

1. Write 00 to Base Address +6h to enable the Run Status register (Base Address +4h).
2. Read the UPD bit (bit 0) to determine whether the DDA-08/16 board being read is the source of the interrupt, as follows:
   - If the UPD bit is 0, the interrupt is from another source. If your PC contains no other DDA-08/16 boards sharing this interrupt, return from the Interrupt Service Routine. If your PC contains other DDA-08/16 boards sharing this interrupt, read the UPD bit of each of these boards, one-at-a-time.
   - If the UPD is 1, this board is the source of the interrupt. The specified analog output channels of this board are updated. Your routine should now load the appropriate DAC input buffers with the data to be clocked out on the next clock cycle.
3. Return from the Interrupt Service Routine.

A

Summary of I/O Address Bits

Table A-1 shows the bit assignments for the read/write, the write only, and the read only registers. Table A-2 summarizes the functions of all bits at the I/O addresses used by DDA-08/16 boards.

Table A-1. Register Bit Assignments

	7	6	5	4	3	2	1	0
Base Address +0h: As Data register (write-only)	D7	D6	D5	D4	D3	D2	D1	D0
As Counter Output register (read/write)	C7	C6	C5	C4	C3	C2	C2	C0
Base Address +1h: As Data register (write-only)	X	X	X	X	D11	D10	D9	D8
As unused	X	X	X	X	X	X	X	X
Base Address +2h (read/write): Data Pointer Register	X	X	X	DP4	DP3	DP2	DP1	DP0
Base Address +4h (read/write): As Run Status register	TRE	GAE	OTR	OON	RCT	X	SWT	UPD
As Board Status register	X	X	X	DOE	SEQ	IL2	IL1	IL0
As Clock Select register	X	X	OP	TRP	GAP	CP	CS1	CS0
As Miscellaneous Status register	PS2	PS1	PS0	X	CLI	GAI	TRI	8/16

Table A-1. Register Bit Assignments (cont.)

	7	6	5	4	3	2	1	0
Base Address +5h: As Control/Status register for Quad DACs 0 and 1 (read/write)	TG1	SP11	SP10	U/B1	TG0	SP01	SP00	U/B0
As Control/Status register for Quad DACs 2 and 3	TG3	SP31	SP30	U/B3	TG2	SP21	SP20	U/B2
As Current/Voltage Switch Status register for Channels 0 to 7 (read-only)	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
As Current/Voltage Switch Status register for Channels 8 to 15 (read-only)	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Base Address +6h: Status Pointer register (read/write)	X	X	X	X	X	X	SP1	SP0

Table A-2. Summary of I/O Address Bits

Bit Name	Description	Page Reference
8/16	The 8/16 board-type bit (bit 0) at Base Address +4h when this register is used as the Miscellaneous Status register	page 1-8
C7 to C0	Bits of Base Address +0h when this register is used for counter read/write data	page 1-3
CH7 to CH0 and CH15 to CH8	Current/Voltage Select registers for channels 0 to 7 and 8 to 15	page 1-11 and page 1-12
CLI	Clock input line bit (bit 3) at Base Address +4h when this register is used as the Miscellaneous Status register	page 1-8
CP	Pacer clock polarity change bit (bit 2) at Base Address +4h when this register is used as the Clock Select register	page 1-7

Table A-2. Summary of I/O Address Bits (cont.)

Bit Name	Description	Page Reference
CS1, CS0	Update clock source select bits (bits 1 and 0) at Base Address +4h when this register is used as the Clock Select register	page 1-7
D0 to D11	Bits of Base Address +0h and +1h when these registers are used for analog output writes	page 1-2
DOE	analog output enable bit (bit 4) at Base Address +4h when this register is used as the Board Status register	page 1-6
DP4 to DP0	Data pointer bits at Base Address +2h	page 1-3
GAE	Gate input enable bit (bit 6) at Base Address +4h when this register is used as the Run Status register	page 1-5
GAI	Gate input line bit (bit 2) at Base Address +4h when this register is used as the Miscellaneous Status register	page 1-8
GAP	Gate polarity selector bit (bit 3) at Base Address +4h when this register is used as the Clock Select register	page 1-7
IL2 to IL0	Interrupt level decode bits (bits 0 to 2) at Base Address +4h when this register is used as the Board Status register	page 1-6
OON	Output clock enable bit (bit 4) at Base Address +4h when this register is used as the Run Status register	page 1-5
OP	Output clock polarity bit (bit 5) at Base Address +4h when this register is used as the Clock Select register	page 1-7
OTR	Output timer run bit (bit 5) at Base Address +4h when this register is used as the Run Status register	page 1-5
PS2 to PS0	Prescaler clock frequency select bit (bits 5 to 7) at Base Address +4h when this register is used as the Miscellaneous Status register	page 1-8
RCT	Pacer clock timer enable bit (bit 3) at Base Address +4h when this register is used as the Run Status register	page 1-5
SEQ	Sequential update of data pointer bit (bit 3) at Base Address +4h when this register is used as the Board Status register	page 1-6
SP1, SP0	Register select bits of the Status Pointer register (Base Address +6h)	page 1-12

Table A-2. Summary of I/O Address Bits (cont.)

Bit Name	Description	Page Reference
SP01, SP00	Analog output 0 voltage span decode bits (bits 1 and 2) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 0 and 1	page 1-9
SP11, SP10	Analog output 1 voltage span decode bits (bits 5 and 6) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 0 and 1	page 1-9
SP21, SP20	Analog output 2 voltage span decode bits (bits 1 and 2) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 2 and 3	page 1-10
SP31, SP30	Analog output 3 voltage span decode bits (bits 5 and 6) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 2 and 3	page 1-10
SWT	Initiate update bit (bit 1) at Base Address +4h when this register is used as the Run Status register	page 1-5
TG0	Analog output 0 update group membership select bit (bit 3) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 0 and 1	page 1-9
TG1	Analog output 1 update group membership select bit (bit 7) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 0 and 1	page 1-9
TG2	Analog output 2 update group membership select bit (bit 3) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 2 and 3	page 1-10
TG3	Analog output 3 update group membership select bit (bit 7) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 2 and 3	page 1-10
TRE	Trigger enable bit (bit 7) at Base Address +4h when this register is used as the Run Status register	page 1-5
TRI	Trigger input line bit (bit 1) at Base Address +4h when this register is used as the Miscellaneous Status register	page 1-8

Table A-2. Summary of I/O Address Bits (cont.)

Bit Name	Description	Page Reference
TRP	Trigger polarity selector bit (bit 4) at Base Address +4h when this register is used as the Clock Select register	page 1-7
U/B0	Analog output 0 unipolar/bipolar mode decode bit (bit 0) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 0 and 1	page 1-9
U/B1	Analog output 1 unipolar/bipolar mode decode bit (bit 4) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 0 and 1	page 1-9
U/B2	Analog output 2 unipolar/bipolar mode decode bit (bit 0) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 2 and 3	page 1-10
U/B3	Analog output 3 unipolar/bipolar mode decode bit (bit 4) at Base Address +5h when this register is used as the Control/Status register for quad analog outputs 2 and 3	page 1-10
UPD	Analog output update bit (bit 0) at Base Address +4h when this register is used as the Run Status register	page 1-5